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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,867	08/06/2003	Hyang-Shik Kong	6192.0157.D1	7649

32605 7590 12/12/2006

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EXAMINER

DUONG, KHANH B

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 12/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/634,867

Applicant(s)

KONG ET AL.

Examiner

Khanh B. Duong

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 November 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 13, 16-22, 24-33, 44 and 47-52 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 19-22, 24-33, 44 and 50 is/are allowed.
- 6) ☒ Claim(s) 13, 16-18, 47-49, 51 and 52 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 21, 2006 has been entered.

Response to Amendment

Accordingly, claims 1, 4-7, 42, 43, 45 and 46 were canceled, claims 13, 19 and 44 were amended, and new claims 49-52 were added.

Currently, claims 13, 16-22, 24-33, 44 and 47-52 are pending in the application.

Response to Arguments

Applicant's arguments with respect to the amended claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 13, 18, 47, 49 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song et al. (US 6,163,356) in view of Kaneko et al. (US 6,433,842).

Song et al. ("Song") discloses in FIG. 4a to 4f a method for manufacturing a thin film transistor array panel, comprising steps of: depositing a first conductive layer formed of an aluminum-based material on a substrate 1; patterning the first conductive layer to form a low-resistance gate line 13a and a low-resistance gate pad 15a connected to the low-resistance gate line 13a; depositing an insulating layer 17 on the low-resistance gate line 13a and the low-resistance gate pad 15a; forming a semiconductor layer (33, 35) on the insulating layer 17; depositing a second conductive layer (21 and 31) on the semiconductor layer (33, 35); patterning the second conductive layer (21 and 31) to form a "data line"; forming a contact hole 59 extending through the insulating layer 17 and exposing the material of a gate pad 15 (formed on the aluminum-based material of the low-resistance gate pad 15a); depositing a third conductive layer formed of an ITO layer; and patterning the third conductive layer to form a conductive pattern 57 directly contacting the material of the gate pad 15 in the contact hole 59 [see col. 4, line 30 to col. 5, line 67].

Re claim 13, Song discloses the ITO layer 57 is formed directly contacting the material (Cr, Mo, Ta or Sb) of the gate pad 15, instead of the aluminum-based material of the low-resistance gate pad 15a. Song further discloses using ITO, instead of indium zinc oxide (IZO) formed by a sputtering process at a temperature below 200°C, to form the conductive pattern directly contacting the gate pad.

Kaneko et al. ("Kaneko") teaches in FIG. 1 forming a second conductive layer 11 formed of indium zinc oxide (IZO) and not directly contacting the aluminum or aluminum alloy material

Art Unit: 2822

of the first conductive layer 8 through the contact hole 19 [see col. 7, line 1 to col. 8, line 65]. By forming the IZO layer 11 and the aluminum or aluminum alloy material layer 8 not directly contacting each other, Kaneko has overcome the known problems associated with high contact resistance that occur when such layers were formed directly contacting each other [see col. 1, lines 30-35]. Thus, Kaneko expressly discloses that IZO (or ITO) has been known to form directly contacting with aluminum or aluminum alloy material in order to exhibit such high contact resistance. Therefore, it is understood that Kaneko discloses a first embodiment that shows an indium zinc oxide (IZO) not directly contacting aluminum or aluminum alloy material layer, and a second embodiment that shows an indium zinc oxide (IZO) directly contacting aluminum or aluminum alloy material layer. Kaneko further teaches the indium zinc oxide (IZO) is formed by a sputtering process at a temperature between room temperature and 200°C [see col. 9, lines 38-43].

Since Song and Kaneko are from the same field of endeavor, the purpose disclosed by Kaneko would have been recognized in the pertinent prior art of Song.

Therefore, it would have been obvious to one of ordinary skill in the art to modify the process of Song by forming an ITO or IZO layer not directly contacting the aluminum or aluminum alloy material layer for the purpose of forming a high resistance gate line. In addition, because ITO and IZO were art-recognized equivalent materials as demonstrated by Kaneko at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute one material for the other. Furthermore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to optimize and select an appropriate temperature for the sputtering process to form the IZO layer. The selection of parameters such

Art Unit: 2822

as energy, power, concentration, temperature, time, depth, thickness, etc., would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. “Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce new and unexpected result which is different in kind and not merely degree from results of prior art ... such ranges are termed ‘critical ranges’ and the applicant has the burden of proving such criticality ... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation”. *In re Aller*, 105 USPQ 233, 235 (CCPA 1955). See also MPEP 2144.05.

Re claim 18, Song expressly discloses in Fig. 4f the step of patterning the third conductive layer comprises a step of forming a pixel electrode 41 connected to the “data line” 31.

Re claim 47, Song discloses in Fig. 4c the insulating layer 17 comprises of silicon oxide or silicon nitride [see col. 4, lines 51-53].

Re claim 49, see discussion above regarding claim 13.

Re claim 51, see discussion above regarding claim 47.

Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song and Kaneko as applied to claims 13, 18, 47, 49 and 51 above, and further in view of Arai et al. (US 6,399,222).

Re claims 16 and 17, Song and Kaneko do not specifically mention the third conductive layer (IZO) being formed by sputtering target including In_2O_3 and ZnO , wherein the content of Zn in a compound of In_2O_3 and ZnO is in the range of 15-20%.

Arai et al. ("Arai") suggests the indium zinc oxide is preferably formed by sputtering target including In_2O_3 and ZnO , wherein the content of Zn in a compound of In_2O_3 and ZnO is in the range of 1-20% [see col. 4, lines 22-32].

Since Song, Kaneko and Arai are from the same field of endeavor, the purpose disclosed by Arai would have been recognized in the pertinent prior art of Song and Kaneko.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined process of Song and Kaneko as suggested by Arai, since Arai states at column 4, lines 47-49 that such modification would provide an electrode layer having a sufficient thickness.

Furthermore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to optimize and select an appropriate content of Zn in a compound of In_2O_3 and ZnO within the range as taught by Arai. The selection of parameters such as energy, power, concentration, temperature, time, depth, thickness, etc., would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes

Art Unit: 2822

such as these may be impart patentability to a process if the particular ranges claimed produce new and unexpected result which is different in kind and not merely degree from results of prior art ... such ranges are termed 'critical ranges' and the applicant has the burden of proving such criticality ... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation".

In re Aller, 105 USPQ 233, 235 (CCPA 1955). See also MPEP 2144.05.

Claims 48 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song and Kaneko as applied to claims 13, 18, 47, 49 and 51 are above, and further in view of Fogarty (US 4,181,564).

Re claims 48 and 52, Song and Kaneko do not disclose depositing the silicon nitride insulating layer at a temperature between about 280°C and about 400°C.

Fogarty et al. ("Fogarty") suggests forming a silicon nitride layer at a temperature between 270°C and 375°C and for a period of about 45 minutes [see col. 2, line 65 to col. 3, line 3 and col. 4, lines 35-55].

Since Song, Kaneko and Fogarty are both from the same field of endeavor, the purpose disclosed by Fogarty would have been recognized in the pertinent prior art of Song and Kaneko.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined process of Song and Kaneko as suggested by Fogarty, since Fogarty states at column 4, lines 26-29 such modification would provide a silicon nitride layer having an essentially constant Si/N ratio throughout the thickness of the layer.

Allowable Subject Matter

Claims 19-22, 24-33, 44 and 50 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: none of the prior art of record, taken alone or in combination, fairly shows or suggests all the limitations as claimed.

Re claim 19, none of the prior art of record discloses the following limitations in combination with the rest of the limitations in the claim: forming a contact hole extending through the passivation layer and the gate insulating layer and exposing the aluminum or aluminum alloy material of the gate pad; depositing a third conductive layer formed of an indium zinc oxide (IZO) layer over the passivation layer; and patterning the third conductive layer to form a redundant gate pad directly contacting the aluminum or aluminum alloy material of the gate pad through the contact hole.

Re claim 44, none of the prior art of record discloses the following limitations in combination with the rest of the limitations in the claim: forming a contact hole extending through the insulating layer and exposing the aluminum or aluminum alloy material of the gate pad; depositing a third conductive layer formed of an indium zinc oxide (IZO) layer; and patterning the third conductive layer to form a conduction pattern directly contacting the aluminum or aluminum alloy material of the gate pad in the contact hole, further comprising, preheating the passivation layer, the silicon nitride layer and the exposed gate pad before the forming the third conductive layer.

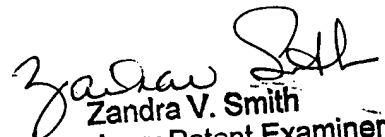
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh B. Duong whose telephone number is (571) 272-1836. The examiner can normally be reached on 10:00-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


KBD


Zandra V. Smith
Supervisory Patent Examiner
11 Dec. 2006